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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re application of: OOI et al.
Serial No.: 09/802,084
Filed: 3/08/01
For: QUANTUM WELL INTERMIXING

Group No.:

Examiner:

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Attached please find the certified copy of the foreign application from which priority is claimed for this case:

Country	**: Singapore**
Application Number	**: PCT/SG00/00038**
Filing Date	**: 8 March 2000**

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REGISTRY OF PATENTS
SINGAPORE

This is to certify that the annexed is a true copy of the following Singapore patent application as filed in this Registry.

Date of Filing	:	08 MAR 2000
Application number	:	PCT/SG00/00038
Applicants	:	NANYANG TECHNOLOGICAL UNIVERSITY
Title of Invention	:	MULTIPLE BANDGAP PHOTONIC INTEGRATION

I further certify that the annexed documents are not, as yet, open to public inspection.

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10 March 2001

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PCT REQUEST

TC5000606WOF

Original (for **SUBMISSION**) - printed on 07.03.2000 03:08:47 AM

0 0-1	**For receiving Office use only** International Application No.	PCT/SG 00 / 00038
0-2	International Filing Date	08 MAR 2000 (08-03-00)
0-3	Name of receiving Office and "PCT International Application"	REGISTRY OF PATENTS (SINGAPORE) PCT INTERNATIONAL APPLICATION
0-4 0-4-1	**Form - PCT/RO/101 PCT Request** Prepared using	PCT-EASY Version 2.90 (updated 01.01.2000)
0-5	**Petition** The undersigned requests that the present international application be processed according to the Patent Cooperation Treaty	
0-6	**Receiving Office (specified by the applicant)**	Intellectual Property Office of Singapore (RO/SG)
0-7	**Applicant's or agent's file reference**	TC5000606WOF
I	**Title of invention**	MULTIPLE BANDGAP PHOTONIC INTEGRATION
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IV-1	**Agent or common representative; or address for correspondence** The person identified below is hereby/has been appointed to act on behalf of the applicant(s) before the competent International Authorities as:	agent
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V	**Designation of States**	
V-1	Regional Patent (other kinds of protection or treatment, if any, are specified between parentheses after the designation(s) concerned)	EP: AT BE CH&LI CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE and any other State which is a Contracting State of the European Patent Convention and of the PCT
V-2	National Patent (other kinds of protection or treatment, if any, are specified between parentheses after the designation(s) concerned)	CA JP KR SG US
V-5	**Precautionary Designation Statement** In addition to the designations made under items V-1, V-2 and V-3, the applicant also makes under Rule 4.9(b) all designations which would be permitted under the PCT except any designation(s) of the State(s) indicated under item V-6 below. The applicant declares that those additional designations are subject to confirmation and that any designation which is not confirmed before the expiration of 15 months from the priority date is to be regarded as withdrawn by the applicant at the expiration of that time limit.	
V-6	**Exclusion(s) from precautionary designations**	NONE
VI	**Priority claim**	NONE
VII-1	**International Searching Authority Chosen**	European Patent Office (EPO) (ISA/EP)

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VIII	Check list	number of sheets	electronic file(s) attached
VIII-1	Request	4	-
VIII-2	Description	11	-
VIII-3	Claims	3	-
VIII-4	Abstract	1	abstract.txt
VIII-5	Drawings	7	-
VIII-7	TOTAL	26	
	Accompanying items	paper document(s) attached	electronic file(s) attached
VIII-8	Fee calculation sheet	✓	-
VIII-9	Separate signed power of attorney	✓	-
VIII-16	PCT-EASY diskette	-	diskette
VIII-18	**Figure of the drawings which should accompany the abstract**	1	
VIII-19	**Language of filing of the international application**	English	
IX-1	**Signature of applicant or agent**		
IX-1-1	Name (LAST, First)	NAMAZIE, Farah	

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10-1	**Date of actual receipt of the purported international application**	~~PCT/SG 00/00038~~ 08 MAR 2000 (08 03 00)
10-2	**Drawings:**	
10-2-1	Received	
10-2-2	Not received	
10-3	**Corrected date of actual receipt due to later but timely received papers or drawings completing the purported international application**	
10-4	**Date of timely receipt of the required corrections under PCT Article 11(2)**	
10-5	**International Searching Authority**	ISA/EP
10-6	**Transmittal of search copy delayed until search fee is paid**	

FOR INTERNATIONAL BUREAU USE ONLY

11-1	**Date of receipt of the record copy by the International Bureau**	

MULTIPLE BANDGAP PHOTONIC INTEGRATION

Field of the Invention

The present invention relates to a method of manufacturing a photonic integrated circuit by quantum well intermixing and to a photonic integrated circuit.

Background of the Invention

The growth of Internet traffic, multimedia services and high-speed data services has exerted pressure on telecommunication carriers to expand the capacity of their networks quickly and cost effectively. The three options normally available are:

1) install new fibers,

This has problems due to costs and difficulties of rights of way.

2) increase the bit rate of the transmission system.

This option is provides inherently limited growth potential.

3) employ wavelength division multiplexing.

This third option allows manifold increase of the network capacity at a modest cost.

Wavelength division multiplexing, also known as frequency division multiplexing, provides an easy way to make use of the available bandwidth by carrying many optical transmission channels together over a single fiber with each channel operating at a different wavelength, or sometimes with data being sent in packets at different frequencies or wavelengths. Carrying signals on a fiber using m wavelengths is equivalent to carrying signals on m strands of fiber using one wavelength per fiber. Apart from capacity expansion, wavelength division multiplexing systems may enable longer span distance between repeaters and the number of spans allowed before regeneration, which make them very attractive for long haul transmission.

The heart of the wavelength division multiplexing systems is a multiple-wavelength laser array, such as a distributed feedback laser array. For known commercial devices, the wavelength of the distributed feedback laser may be tuned by defining gratings with a submicron period to perform frequency chirp. The device grating is conventionally formed by e-beam lithography, as holography is not suitable for creation of complex multi-pitch grating structures. E-beam writers for performing such electron beam lithography are however costly and of low throughput. Thus electron beam lithography is not favorable for large-scale device production. In addition, regrowth of the sample is necessary, and this entails additional cost.

Alternatively selective area epitaxial growth has been used to fabricate multiple wavelength lasers. This technique utilizes differences in epitaxial layer composition and thickness produced by growth through a mask to achieve spatially selective bandgap variation. This process works well under a precisely controlled set of parameters but is difficult to manipulate in a generic fashion.

By applying a gray mask technique using quantum well intermixing by impurity-induced disordering, the bandgap energy of a quantum well material can be tuned to different degrees across a wafer using only one lithography and implantation process step. This enables not only the integration of monolithic multiple-wavelength lasers but to further extends to integrate with modulators and couplers on a single chip.

It is believed that the impurity-induced disordering technique has not been used in full production although two research groups have successfully produced monolithic multiple-wavelength lasers using the technique. One group has produced

four channel lasers in 1.3 μm InGaAs/InP quantum well material using high energy (2 MeV) P implantation. The second has produced 2-channel lasers in 1.55 μm InGaAs/InGaAsP quantum well material using low energy P implantation.

By means of the invention, monolithic integration of multiple-wavelength lasers in, for example, 1.55 μm InGaAs/InGaAsP materials with more than 5 channels using low energy IID process is possible.

It is generally accepted as desirable to integrate together photonic and optoelectronic components onto a single chip. The reasons for this are the ability to obtain high device yields and overall improvements in performance, reliability and robustness and a general reduction in cost.

A major aim in fabricating monolithic photonic integrated circuits is to be able to control the bandgap energy across the semiconductor wafer. The absorption band edge of quantum well structures is desirably controlled across the wafer to allow for fabrication of integrated lasers, modulators and low loss waveguides. Bandgap control has been attempted in the prior art by a number of techniques, for example by etching and regrowth on bulk material, by selective area epitaxy or by using quantum well intermixing techniques including impurity induced disordering and impurity-free vacancy disordering.

Each of the methods of the prior art has disadvantages. For example, using etching and regrowth methods results in poor optical confinement to the waveguide devices. As it involves multiple processing steps there is often a low yield and throughput may be low.

Selective area epitaxy is also a complicated technique and requires complex steps of sample preparation. Also, the

technique may give non-uniform growth rate across the strip which prevents subsequent planar processing. For the same reason, passive waveguide sections may be relatively lossy.

Quantum well intermixing can be used selectively to modify the bandgap energy of a quantum well sample. However, spatial control of the bandgap using the prior art quantum well intermixing techniques is complicated. For example using varying thicknesses of silicon dioxide layers as intermixing sources of impurity-free vacancy disordering, or implant masks for impurity induced disordering increases the number of processing steps of lithography and deposition of dielectric caps.

To overcome this complexity the prior art includes a one-step spatially controlled quantum well intermixing technique based upon impurity-free vacancy disordering. In this process, the semiconductor is patterned with very small areas of SrF_2 followed by coating the sample with SiO_2. The degree of intermixing then depends on the area of semiconductor substrate in direct contact with the SiO_2 layer. This technique, although being one-step, requires electron beam lithography which decreases the process throughput and increases design complexity.

It is accordingly an object of the present invention to at least partially mitigate the difficulties of the prior art.

Summary of the Invention

According to a first aspect of the present invention there is provided a method of manufacturing a photonic integrated circuit comprising providing a structure having a quantum well region, and performing quantum well intermixing, characterized in that said step of performing quantum well intermixing comprises differentially masking portions of said region,

implanting impurities into said differentially masked portions and annealing said structure.

Preferably said step of differentially masking portions of said region comprises forming a masking layer on said portion of said region and differentially etching said masking layer.

Advantageously before said etching step the method comprises forming a photoresist on said masking layer, applying

Conveniently said step of applying photoresist may comprise spin-coating said photoresist.

Conveniently said masking layer comprises a dielectric such as silicon dioxide. Alternatively said masking layer may comprise a polymer or a metal.

Conveniently said masking layer comprises silicon dioxide.

Preferably said etching step comprises dry etching.

Advantageously said dry etching has a one-to-one selectivity between photoresist and said masking layer.

Conveniently process parameters of a dry etching system are selected to provide said one-to-one selectivity.

Conveniently said annealing step is performed in a rapid thermal processor, alternatively a rapid thermal annealer or furnace may be used.

Preferably said impurities comprise phosphorus.

According to a second aspect of the present invention there is provided a photonic integrated circuit comprising plural laser

devices, each laser device having a mutually different wavelength in use, each laser device comprising a quantum well region wherein said different wavelengths are achieved by quantum well intermixing produced by differentially masking said integrated circuit, introducing impurities into said differentially masked regions and annealing the integrated circuit.

Brief Description of the Drawings

An exemplary embodiment of the invention will now be described with reference to the accompanying drawings in which:-

Figure 1 shows an exemplary process flow for fabrication of multiple wavelength lasers;

Figure 2 shows in diagrammatic form a quantum well structure used in the present invention and the bandgap variation of that structure;

Figure 3 is a table of optical densities for the gray masks used in the embodiment.

Figure 4 shows the thickness of resist and oxide before and after reactive ion etching;

Figure 5 shows a schematic diagram of a multi-channel monolithic laser;

Figure 6 shows the lasing spectra observed from the chip and;

Figure 7 shows the threshold current comparison between non-implanted and direct implanted regions.

Description of the Preferred Embodiments

Referring first to Figure 1, an outline of the process of the invention will now be given:-

In step (i) laser isolation and alignment mark etching is performed for example using a first mask having a 20μm stripe pattern. This etching process is for example a wet-etching process with an exemplary etchant of sulphuric acid, hydrogen peroxide and water in 1:8:40 ratio whereby 0.15μm of the InGaAs and InGaAsP contact layer is removed (100).

The structure 101 is then coated with oxide 102 after the wet etching and then a positive photo resist 103 is spin-coated onto the structure. In step (ii), photolithography is carried out to transfer the gray patterns onto the structure. In step iii, a dry etching process, is performed so as to etch correspondingly into the oxide so that different thicknesses (104, 105, 106) of oxide are produced in correspondence with the gray masking.

It will be understood that masks other than oxide could be used, for example, polymer, metal or photoresist mask materials, or dielectrics other than oxide.

In step iv, implantation is carried out with impurity ions, such as phosphorus, the degree of implantation being inverse to the thickness of the graded masks (104-106).

After implantation, in step v, annealing is carried out for quantum well intermixing, followed by testing and measurement - step vi.

In more detail, and referring to Figure 2, an In_xGa_{1-x} As/$In_xGa_{1-x}As_yP_{1-y}$ structure (10) was grown using metal organic chemical vapour deposition (MOCVD) on a lower InP cladding layer (12) on an InP substrate. A single undoped quantum well region (14) was formed, consisting of a 5.5 nm wide $GaIn_xAs$ QW, with

12 nm $GaIn_xAs_yP$ (λ_g=1.26μm) barriers (16,18). The active region was bounded by step graded index (GRIN) $GaIn_xAs_yP$ confining layers (20-2, 24-6). The thickness and composition of these layers were 50nm of λ_g=1.18 μm and 80nm of λ_g=1.05 μm, respectively. The structure, which was lattice matched to InP throughout, was completed with a 1.4 μm InP upper cladding layer (28) and a layer (30) of 0.65 μm $GaIn_xAs_yP$ followed by a 0.1μm $GaIn_xAs$ layer (32) forming a contact layer. The lower cladding layer (12) was Sulphur-doped to a concentration of $2.5x10^{18}$ cm^{-3}. The upper cladding layer (28) was doped with Zn to a concentration of $7.4x10^{17}$ cm^{-3} and the subsequent layers (30,32) were doped with $2x10^{18}$ cm^{-3} and $1.3x10^{19}$ cm^{-3} concentration of Zn respectively. The core of the waveguide was undoped, thus forming a P-I-N structure with its intrinsic region restricted to the quantum well and GRIN layers.

Simulations of the P-implantation ranges and vacancy distribution were first carried out to determine the thickness of SiO_2 required to obtain the bandgap shift which was sought. It would alternatively be possible to use other theoretical calculations. In the present case, the thickness of SiO_2 mask required to totally block P ions from reaching the semiconductor during implantation was found to be 900 nm.

The gray mask technique of the invention makes use of different transparency of masks to control the degree of the exposure of photoresist at selected regions and thus different thickness of photoresist after development. The degree of the development of photoresist after UV exposure has a linear relationship with the optical density. In one embodiment, the gray mask was designed to have 10 levels for multiple wavelength lasers, i.e. from 0.15 to 1.05 with a step of 0.5, of optical density, see Figure 4. By this means, 10 different bandgaps were obtained across the sample after quantum well intermixing. It will of course be clear to those skilled in

the art that fewer or greater numbers of bandgaps could be provided, according to the requirements of the application.

The relationship between optical density of mask and the UV light transmissivity level during lithography process can be expressed using the following equation.

$OD = -\log (T)$

where OD is optical density and T is transmissivity.

A reactive ion etching process with 1:1 selectivity between photoresist and SiO_2 was used to transfer various thickness of photoresist to the SiO_2 layer. This process was performed in a conventional parallel plate radio-frequency reactive ion etching system using CF_4 and O_2 as process gases. Taguchi's optimisation approach, a statistical method used in industrial process optimisation, has been employed to optimise the parameters of this novel non-selective reactive ion etching process. To achieve 1:1 non-selective etching, the following settings were found suitable for the particular materials in question: pressure of 100 mTorr, RF power 60W, CF_4 flow rate 60 sccm and O_2 flow rate 2scccm. After reactive ion etching, the samples were implanted with $1x10^{14}$ cm^{-2} at 360 keV, at 200°C. The quantum well intermixing process was completed by annealing using a rapid thermal processor at 590 °C for 120s. Broad area guided lasers were then fabricated on the samples. The lasers were then cleaved and tested under pulsed conditions.

The thickness of the resist and SiO_2, as measured from a surface profiler, both before and after RIE for the sample is given in Figure 4. It will be seen that smooth and obvious transitions at each transmitivity level have been obtained.

After fabrication, multiple wavelength lasers were cleaved from the rows of multiple wavelength lasers for light versus current and spectrum measurements. An exemplary schematic

diagram of a monolithic laser having 4-channel multiple wavelengths is shown in Figure 5. The spectrum and light versus current measurements were carried out under pulsed current conditions at room temperature. The current pulsed width was 3.5 μs and the repetition frequency was 100 KHz (35% of duty cycle).

Monolithic multiple wavelength lasers fabricated using this gray mask technique were observed to operate at 10 distinctive wavelengths of 1.558μm, 1.555 μm, 1.548 μm, 1.543 μm, 1.532 μm, 1.515 μm, 1.487 μm, 1.480 μm, and 1.484 μm respectively (Fig. 6).

From Figure 7, only a 15 % increase of threshold current density between the non-implanted (Gray 1: full oxide, not intermixed but annealed) and direct implanted (Gray 10: no oxide, fully intermixed and annealed) regions. Furthermore, the slope efficiency shows very little change: this indicates that the quality of the materials remains high after intermixing using this technique. The technique may be used to produce multi-frequency devices as well as other components since the material produced by this technique is of relatively high electrical and optical quality. Thus the technique is suited to the production of photonic integrated circuits.

Although the present invention has been described using a specific compound semiconductor, it is applicable to other compound semiconductors. The embodiment has been described using oxide as the mask but it will be understood by those skilled in the art that any suitable dielectric can be used or indeed that a polymer or metal mask can be used instead. In the described embodiment a mask was used as well as a photoresist but it will also clear to those skilled in the art that a graded photoresist could be used without an additional mask. The embodiment has been described in the context of a

rapid thermal processor but rapid thermal annealers, furnaces and other temperature devices may be used instead.

CLAIMS:

1. A method of manufacturing a photonic integrated circuit comprising providing a structure having a quantum well region, and performing quantum well intermixing, characterised in that said step of performing quantum well intermixing comprises differentially masking portions of said region, implanting impurities into said differentially masked regions, and annealing said structure.

2. The method of claim 1, wherein said step of differentially masking portions of said region comprises forming a masking layer on said portion of said region and differentially etching said masking layer.

3. The method of claim 2 wherein, before said etching step, the method comprises forming a photoresist on said masking layer, applying masks having different optical densitites to said photoresist and developing said photoresist.

4. The method of claim 3, wherein said step of applying photoresist comprises spin-coating said photoresist.

5. The method of any of claims 2-4 wherein said masking layer comprises a dielectric .

6. The method of claim 5, wherein said dielectric is silicon dioxide.

7. The method of any of claims 2-4, wherein said masking layer comprises a polymer.

8. The method of any of claims 2-4, wherein said masking layer comprises a metal.

9. The method of claim 2 wherein said etching step comprises dry etching.

10. The method of claim 9, wherein said dry etching has a one-to-one selectivity between photoresist and said masking layer.

11. The method of claim 10, wherein process parameters of a dry etching system are selected to provide said one-to-one selectivity.

12. The method of claim 1 or claim 2, wherein said step of differentially masking portions of said region comprises using a graded photoresist.

13. The method of any preceding claim, wherein said step of implanting impurities comprises ion implantation.

14. The method of any of claims 1-12 wherein said step of implanting impurities comprises a focused ion beam technique.

15. The method of any of claims 1-12, wherein said step of implanting impurities comprises diffusion.

16. The method of any preceding claim wherein said annealing step is performed in a rapid thermal processor.

17. The method of any of claims 1-15, wherein said annealing step uses a rapid thermal annealer.

18. The method of any of claims 1-15, wherein said annealing step is performed in a furnace.

19. The method of any preceding claim wherein said impurities comprise phosphorus.

20. A photonic integrated circuit comprising plural laser devices, each laser device having a mutually different wavelength in use, each laser device comprising a quantum well region wherein said different wavelengths are achieved by quantum well intermixing produced by differentially masking said integrated circuit, introducing impurities into said differentially masked regions and annealing the integrated circuit.

ABSTRACT

MULTIPLE BANDGAP PHOTONIC INTEGRATE CIRCUIT

A photonic integrated circuit is produced by performing quantum well intermixing of a quantum well structure, the intermixing being carried out by implanting impurities through differential masks into the circuit and annealing it. The masks are produced by differential density layers.

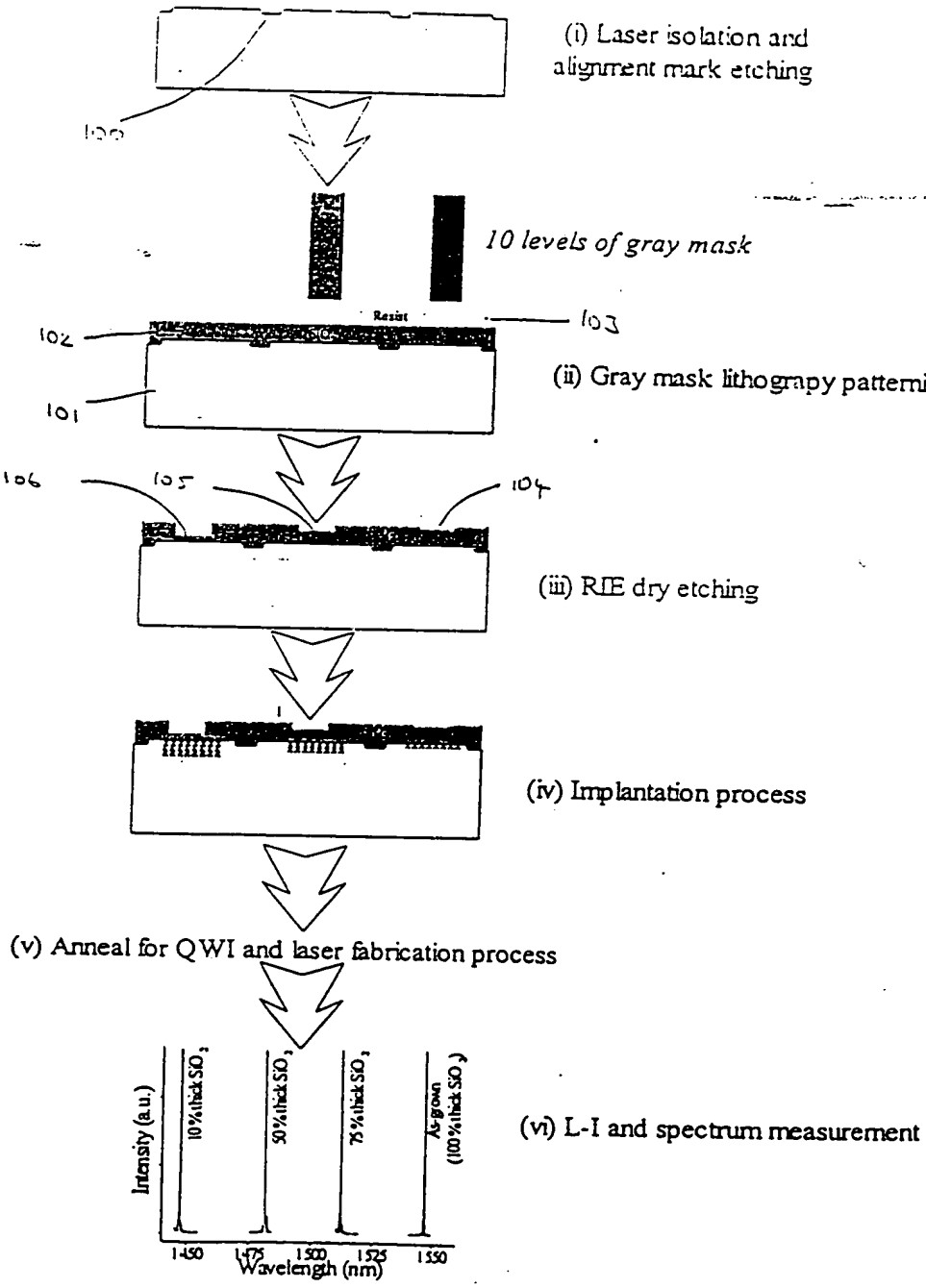
(i) Laser isolation and alignment mark etching
100
10 levels of gray mask
Resist
103
102
101
(ii) Gray mask lithograpy patterning
106
105
104
(iii) RIE dry etching
(iv) Implantation process
(v) Anneal for QWI and laser fabrication process
Intensity (a.u.)
10% thick SiO2
50% thick SiO2
75% thick SiO2
As-grown (100% thick SiO2)
1450
1475
1500
1525
1550
Wavelength (nm)
(vi) L-I and spectrum measurement

FIG. 1

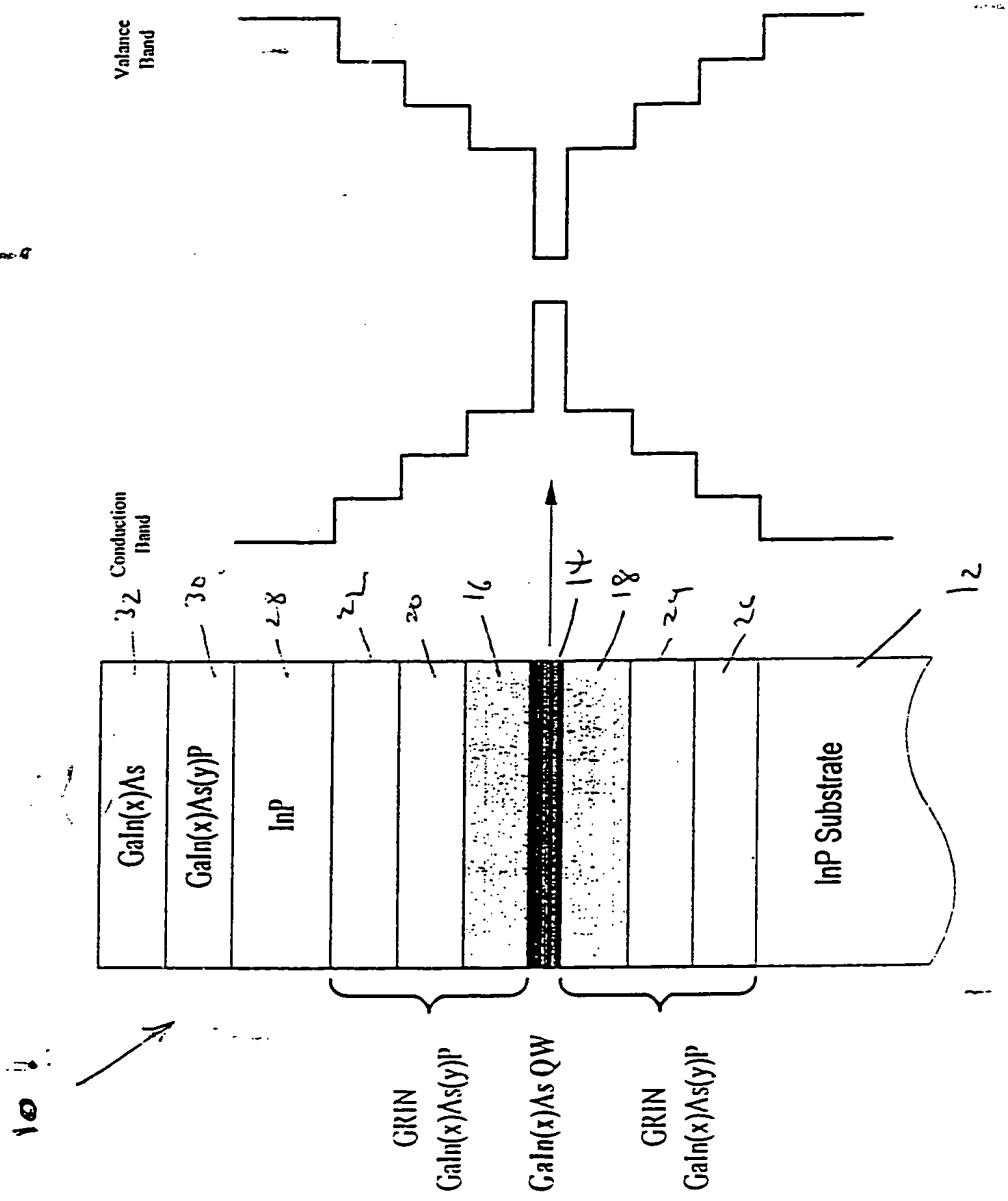
Valance Band
Conduction Band
Bandgap Energy
Layer Structure
GaIn(x)As
GaIn(x)As(y)P
InP
InP Substrate
GRIN GaIn(x)As(y)P
GaIn(x)As QW
GRIN GaIn(x)As(y)P
10
12
14
16
18
20
22
24
26
28
30
32

FIG. 2

	Gray Level									
	1	2	3	4	5	6	7	8	9	10
OD	0.15	0.25	0.35	0.45	0.55	0.65	0.75	0.85	0.95	1.05
T (%)	70.8	56.2	44.7	35.5	28.2	22.4	17.8	14.1	11.2	8.9

FIG. 3

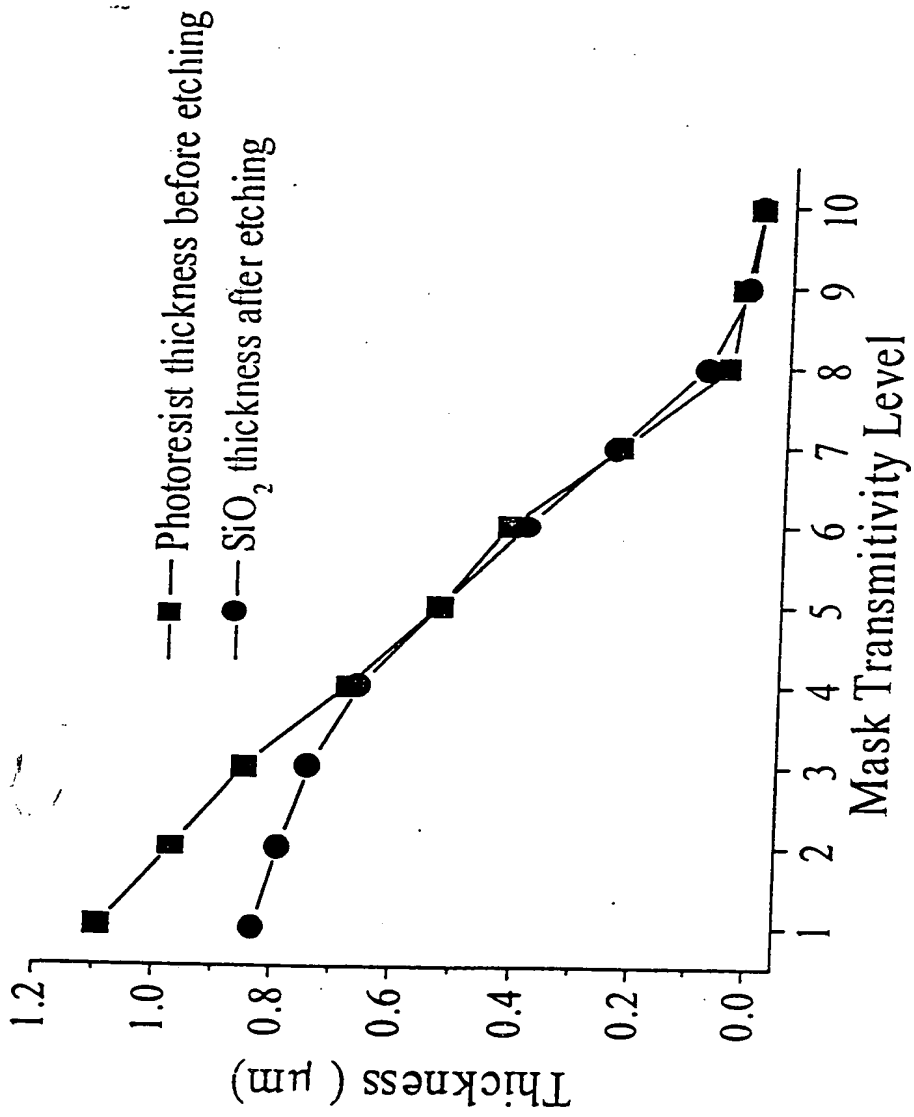
Photoresist thickness before etching
SiO_2 thickness after etching
Thickness (μm)
1.2
1.0
0.8
0.6
0.4
0.2
0.0
1
2
3
4
5
6
7
8
9
10
Mask Transmitivity Level

FIG. 4

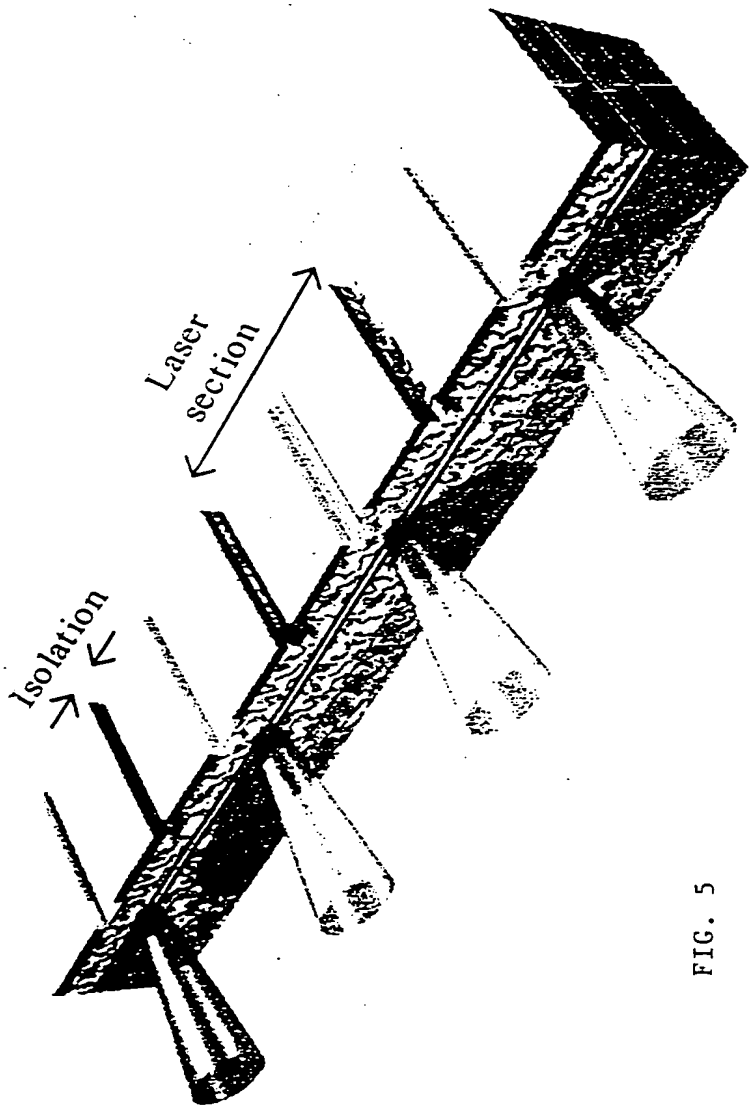

FIG. 5

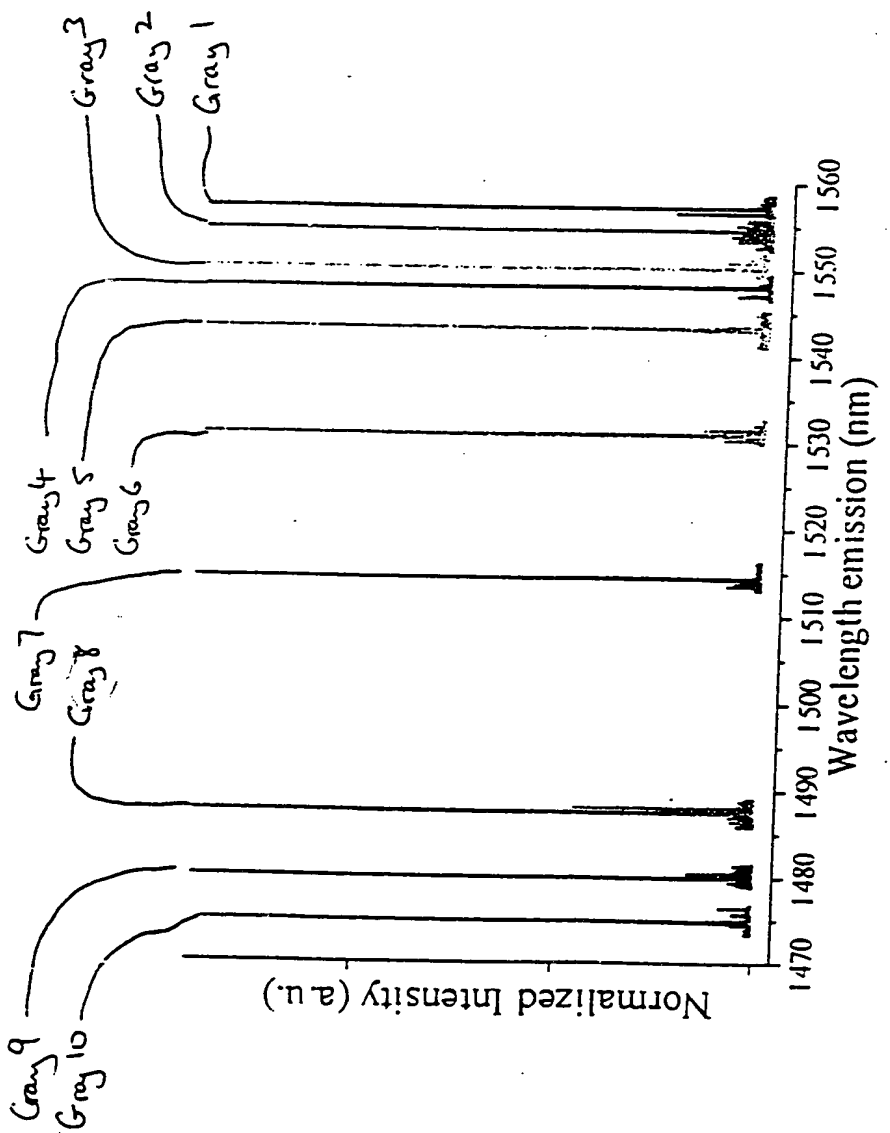
Gray 3
Gray 2
Gray 1
Gray 4
Gray 5
Gray 6
Gray 7
Gray 8
Gray 9
Gray 10
Normalized Intensity (a.u.)
1470
1480
1490
1500
1510
1520
1530
1540
1550
1560
Wavelength emission (nm)

FIG. 6

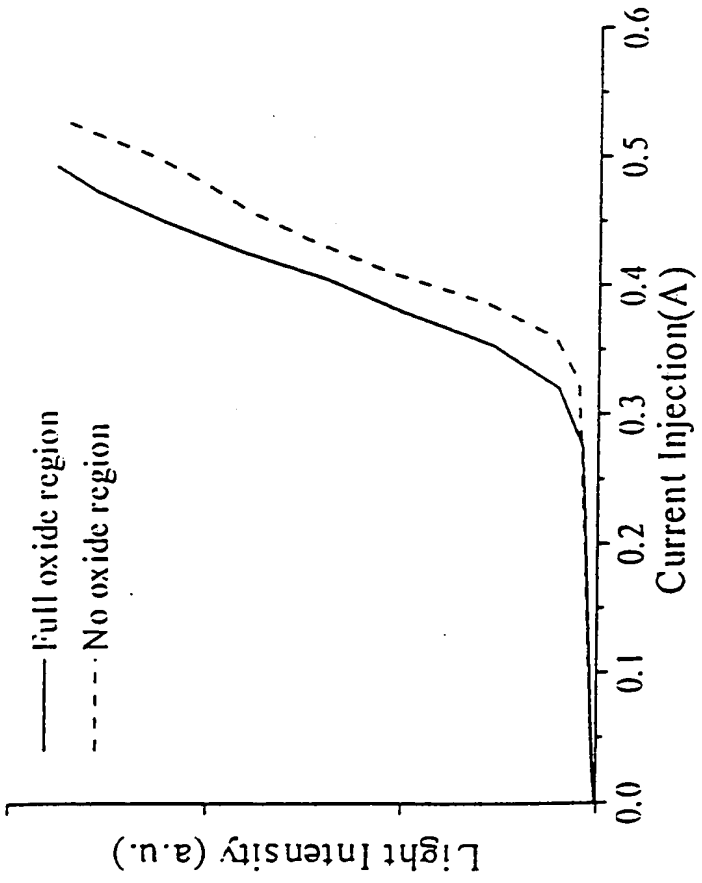
Full oxide region
No oxide region
Light Intensity (a.u.)
0.0
0.1
0.2
0.3
0.4
0.5
0.6
Current Injection(A)

FIG. 7